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**BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES**

Application Number: 10/751,440
Filing Date: January 06, 2004
Appellant(s): ALTICE, PETER PARKER

Thomas J. D'Amico
David T. Beck
For Appellant

**EXAMINER'S ANSWER**

This is in response to the appeal brief filed September 22, 2008 appealing from the Office action mailed January 28, 2008.

**(1) Real Party in Interest**

A statement identifying by name the real party in interest is contained in the brief.

**(2) Related Appeals and Interferences**

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

**(3) Status of Claims**

The statement of the status of claims contained in the brief is correct.

**(4) Status of Amendments After Final**

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

**(5) Summary of Claimed Subject Matter**

The summary of claimed subject matter contained in the brief is correct.

**(6) Grounds of Rejection to be Reviewed on Appeal**

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

**(7) Claims Appendix**

The copy of the appealed claims contained in the Appendix to the brief is correct.

**(8) Evidence Relied Upon**

| | | |
|---|---|---|
| 7,281,174 | Weale et al. | 10-2007 |
| 6,710,804 | Guidash | 03-2004 |
| 6,160,281 | Guidash | 12-2000 |
| 6,069,376 | Merriill | 05-2000 |
| 2003/0090575 | Miyamoto | 05-2003 |

**(9) Grounds of Rejection**

The following ground(s) of rejection are applicable to the appealed claims:

Claims 1, 2, 4, 6, 9, 10-12, 14, 16, 19, 20-23, 25, 27-34 rejected under 35 U.S.C. 103(a) as being unpatentable over Weale (US 7,286,174 B1) in view of Guidash (US 6,710,804 B1).

As to claim 1, Weale discloses, in Figure 1, a pixel cell, comprising:

- a first storage node (120) for storing charge generated at a photosensitive element (112) during an integration period; and
- a second storage node (140) for storing a portion of said charge generated by said photosensitive element during the integration period that is not stored by said first storage node (col. 3, lines 42-53),

but does not teach wherein the charges are stored prior to storing said charge at a floating diffusion region.

Guidash teaches, in Figure 1b and 2, transferring charges to a floating diffusion region (18) (col. 4, lines 17-20).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have used the structure of the pixel cell, specifically the floating diffusion region of Guidash, with the dual storage node pixel cell of Weale in order to provide extended dynamic range and high sensitivity to incident light. (See col. 2, lines 6-9 of Guidash.)

As to claim 2, Weale wherein said photosensitive element is a photodiode (112; col. 4, line 29).

As to claim 4, Weale teaches wherein said first storage node comprises a storage capacitor (122; col. 3, line 67).

As to claim 6, Weale teaches wherein said second storage node comprises a storage capacitor (142; col. 4, line 3).

As to claim 9, Weale teaches, in Figure 1, a pixel cell further comprising a first transfer transistor (162) switchably coupled between at least one of said first and second storage nodes and said floating diffusion region (col. 4, lines 34-41).

As to claim 10, Weale teaches, in Figure 5, a pixel cell further comprising:

- a first transfer transistor (262) switchably coupled between said first storage node and said floating diffusion region; and
- a second transfer transistor (272) switchably coupled between said second storage node and said floating diffusion region (col. 11, lines 33-40).

As to claims 11, 12, 14, 16, 19, and 20, these claims only differ from claims 1, 2, 4, 6, 9, and 10 in that claims 11, 12, 14, 16, 19, and 20 claim a semiconductor chip comprising a plurality of pixels (Weale discloses a pixel array (col. 19, line 52) and a semiconductor chip (col. 5, lines 53-54)), each pixel having the same configuration as claimed in claims 1, 2, 4, 6, 9, and 10. Thus, claims 11, 12, 14, 16, 19, and 20 are analyzed as previously discussed in claims 1, 2, 4, 6, 9, and 10.

As to claim 21, Weale and Guidash teach the limitations of claim 11; Guidash further teaches the chip further comprising a sample and hold circuit for receiving said charge stored by said floating diffusion region (Fig. 1B, col. 3, line 62- col. 4, line 13)

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have used the sample and hold circuit of Guidash to transfer charges to the floating diffusion region of Weale and Guidash to provide extended dynamic range and high sensitivity to incident light. (See col. 2, lines 6-9 of Guidash.)

As to claim 22, Guidash teaches wherein said sample and hold circuit comprises at least four storage nodes, each respectively for storing a reset voltage and a signal voltage representing a charge stored by each of said first and second storage nodes (C5 and C6, Fig. 1b of Guidash, col. 4, lines 46-51).

As to claim 23, Guidash teaches wherein said sample and hold circuit further comprises at least two storage nodes (C5 and C6 of Guidash) for respectively storing a reset voltage of said floating diffusion region and a signal voltage of at least one of said first and second storage nodes (col. 4, lines 46-51).

As to claim 25, Weale teaches, in Figure 1, a method for operating an image sensor, the method comprising:

- receiving, at a first storage node (120) of a pixel cell, charge generated by a photosensitive element (112) of said pixel cell during an integration period (col. 3, lines 42-53);
- receiving, at a second storage node (140) of said pixel cell, a portion of said charge generated by said photosensitive element during the integration period not stored at said first storage node (col. 3, lines 42-53);

but does not teach:

- transferring said charge to a floating diffusion regision of said pixel cell.

Guidash teaches

- transferring said charge from to a floating diffusion region (18) of said pixel cell (col. 4, lines 17-20 of Guidash).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have used the structure of the pixel cell, specifically the floating diffusion region of Guidash, with the dual storage node pixel cell of Weale in order to provide extended dynamic range and high sensitivity to incident light. (See col. 2, lines 6-9 of Guidash.)

As to claim 27, Weale teaches wherein said second act of receiving comprises receiving said portion of said charge at a storage capacitor (142) of said pixel cell (col. 4, line 3).

As to claim 28, Weale teaches wherein said act of transferring comprises:

- transferring said charge from said first storage node (120) (col. 3, lines 51-53) and to a column line associated with said pixel cell (Fig. 1; output is readout to the column bus);

but does not teach:

- transferring charges to a floating diffusion region.

Guidash teaches:

- transferring charges to a floating diffusion region (col. 2, lines 6-9).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have used the structure of the pixel cell, specifically the floating diffusion region of Guidash, with the dual storage node pixel cell of Weale in order to provide extended dynamic range and high sensitivity to incident light. (See col. 2, lines 6-9 of Guidash.)

As to claim 29, Weale teaches wherein said act of transferring comprises:

- transferring said charge from said second storage node (140) (col. 3, lines 51-53) and to a column line associated with said pixel cell (Fig. 1; output is readout to the column bus);

but does not teach:

- transferring charges to a floating diffusion region.

Guidash teaches:

- transferring charges to a floating diffusion region (col. 2, lines 6-9).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have used the structure of the pixel cell, specifically the floating diffusion region of Guidash, with the dual storage node pixel cell of Weale in order to

provide extended dynamic range and high sensitivity to incident light. (See col. 2, lines 6-9 of Guidash.)

As to claim 30, Weale teaches wherein said first act of receiving comprises activating a shutter gate transistor (first charge transfer gate 124) coupled between said first storage node and said photosensitive element (Fig. 1, col. 3, line 67-col. 4, line 2).

As to claim 31, Weale teaches wherein said second act of receiving comprises activating a shutter gate transistor (second charge transfer gate 144) coupled between said - second storage node and said photosensitive element (Fig. 1, col. 3, line 67-col. 4, 2).

As to claim 32, Weale teaches wherein said act of transferring comprises activating a transfer transistor (buffer 162) coupled between at least one of said first and second storage nodes and said floating diffusion region (col. 4, lines 34-41).

As to claim 33, Weale teaches a method for operating an image sensor, the method comprising:

- receiving light at a photosensitive element (112) of a first pixel cell during an integration period (col. 4, lines 44-45);
- transferring charge generated during the integration period by said photosensitive element to a first storage node (120) of said first pixel cell;
- transferring a portion of said charge generated during the integration period not transferred to said first storage node to a second storage node (140) of said first pixel cell (col. 3, lines 42-53);

- transferring said charge from said first storage node to an output (col. 4, lines 34-41);
- transferring said charge from said second storage node to an output (col. 4, lines 34-41); and
- reading out said charge (output buffer 162 to column bus 166; Fig. 1);

but does not teach;

- transferring charges to a floating diffusion region of said first pixel;
- reading out said charge from said floating diffusion region.

Guidash teaches

- transferring charges to a floating diffusion region (18) of said first pixel cell (col. 4, lines 17-20);
- reading out said charge from said floating diffusion region (Charge on the floating diffusion is sampled; col. 4, lines 41-44);

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have used the structure of the pixel cell, specifically the floating diffusion region of Guidash, with the dual storage node pixel cell of Weale in order to provide extended dynamic range and high sensitivity to incident light. (See col. 2, lines 6-9 of Guidash.)

As to claim 34, Weale teaches the method of claim 33 further comprising the act of resetting at least one of said photosensitive element and said floating diffusion region (preset gate 116; col. 7, lines 30-39).

Claims 3, 5, 7, 8, 13, 15, 17, 18, and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Weale (US 7,286,174 B1) in view of Guidash (US 6,710,804 B1) as applied to claims 1, 11, and 25 above, and further in view of Merrill (US 6,069,376).

As to claim 3, Weale in view of Guidash teaches the pixel cell of claim 1, but does not teach wherein said first storage node comprises a gated storage node.

Merrill teaches wherein said first storage node comprises a gated storage node (86; col. 7, line 7).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have used the gated storage node of Merrill with the pixel of Weale in view of Guidash to provide a storeage-pixel sensor and an imaging array of storage-pixel sensors that incorporate a “film-speed” switching capability without adding significantly to the layout area of the imaging array. (See col. 2, lines 47-50 of Merrill).

As to claim 5, Merrill teaches wherein said second storage node comprises a gated storage node (col. 7, line 7).

As to claim 7, Merrill teaches wherein said gated storage node comprises (86):

- a depletion area (130) between said photosensitive element and said floating diffusion region (col. 7, lines 58-60); and
- a barrier region (126 ) adjacent to said depletion area (col. 7, lines 54-56).

As to claim 8, Merrill teaches wherein said depletion area and said barrier region comprise oppositely doped silicon (col. 7, lines 54-60).

As to claims 13, 15, 17, and 18, these claims differ only in that these claims claim a semiconductor chip comprising a plurality of pixels (Weale discloses a pixel array (col. 19, line 52) and a semiconductor chip (col. 5, lines 53-54)), each pixel having the same configuration as claimed in claims 3, 5, 7, and 8. Thus, claims 13, 15, 17, and 18 are analyzed as previously discussed in claims 3, 5, 7, and 8.

As to claim 26, Merrill teaches wherein said first act of receiving comprises receiving said charge at a gated storage node (86) of said pixel cell (col. 7, line 7).

Claims 24 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Weale (US 7,286,174 B1) in view of Guidash (US 6,160,281).

As to claim 24, Weale teaches a semiconductor chip (col. 5, lines 53-54), comprising:

- a plurality of pixel cells (col. 19, line 52) comprising:
- a first storage node (120) for storing charge generated at a photosensitive element (112) during an integration period prior to storing said charge on said common floating diffusion region; and
- a second storage node (140) for storing a portion of said charge generated by said photosensitive element during the integration period that is not stored by said first storage node (col. 3, lines 47-51);

but does not teach wherein at least two of which share a common floating diffusion region.

Guidash teaches wherein at least two of which share a common floating diffusion region (84; Fig. 8, col. 4, lines 57-61).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have have used the common floating diffusion region of Guidash with the semiconductor chip of Weale so that layout efficiencies can be utilized to improve the fill factor of the pixel. (See col. 3, lines 1-3 of Guidash (US 6,160,281).)

As to claim 35, Weale teaches the method of claim 33 further comprising:

- receiving light at a second photosensitive element (112) of a second pixel cell (col. 4, lines 44-45);
- transferring charge generated by said second photosensitive element to a first storage node (120) of said second pixel cell;
- transferring a portion of said charge not transferred to said first storage node of said second pixel cell to a second storage node (140) of said second pixel cell (col. 3, lines 42-53);
- transferring said charge from said first storage node of said second pixel cell to an output (col. 4, lines 34-41);
- transferring said charge from said second storage node of said second pixel cell to an output (col. 4, lines 34-41); and
- reading out said charge (output buffer 162 to column bus 166; Fig. 1);

but does not teach wherein said first and second pixel cells share said floating diffusion region and wherein charges are readout from said floating diffusion.

Guidash teaches wherein said first and second pixel cells share said floating diffusion region (84; Fig. 8, col. 4, lines 57-61) and wherein charges are readout from said floating diffusion region (col. 5, lines 1-11).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have have used the common floating diffusion region of

Guidash with the semiconductor chip of Weale so that layout efficiencies can be utilized to improve the fill factor of the pixel. (See col. 3, lines 1-3 of Guidash (US 6,160,281).)

Claims 36, 37, 39, 41, 44, and 45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Weale (US 7,286,174 B1) in view of Guidash (US 6,710,804 B1) and further in view of Miyamoto (US 2003/0090575 A1).

As to claims 36, 37, 39, 41, 44, and 45, these claims differ from claims 1, 2, 4, 6, 9, and 10 only in that a processor is additionally recited. Weale in view of Guidash does not teach a processor. Miyamoto teaches a processor (7; paragraph [0029]).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have used the processor of Miyamoto with the system of Weale as modified by Guidash to provide an electronic still camera which is capable of effecting continuous shooting at a higher speed. (See paragraph [0011] of Miyamoto).

Claims 38, 40, 42, and 43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Weale (US 7,286,174 B1) in view of Guidash (US 6,710,804 B1) as modified by Miyamoto (US 2003/0090575 A1) as applied to claim 36 above, and further in view of Merrill (US 6,069,376).

As to claim 38, Weale in view Guidash as modified by Miyamoto does not teach wherein said first storage node comprises a gated storage node.

Merrill teaches wherein said first storage node comprises a gated storage node (86; col. 7, line 7).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have used the gated storage node of Merrill with the pixel of Weale to provide a storage-pixel sensor and an imaging array of storage-pixel sensors that incorporate a “film-speed” switching capability without adding significantly to the layout area of the imaging array. (See col. 2, lines 47-50 of Merrill).

As to claim 40, Merrill teaches wherein said second storage node comprises a gated storage node (col. 7, line 7 of Merrill).

As to claim 42, Merrill teaches wherein said gated storage node comprises (86 of Merrill):

- a depletion area (130 of Merrill) between said photosensitive element and said floating diffusion region (col. 7, lines 58-60 of Merrill); and
- a barrier region (126 of Merrill) adjacent to said depletion area (col. 7, lines 54-56 of Merrill).

As to claim 43, Merrill teaches wherein said depletion area and said barrier region comprise oppositely doped silicon (col. 7, lines 54-60 of Merrill).

**(10) Response to Argument**

The examiner respectfully disagrees that the rejection should be reversed. Only those actual arguments raised by Appellants are being treated in the Examiner's Answer. Any further arguments regarding other elements or limitation not specifically argued that the appellant could have made are considered by the examiner as having been conceded by the appellant for the basis of the decision of this appeal. Accordingly,

they are not being addressed by the examiner for further consideration by the panel. Each of the remarks and or arguments filed with the appeal brief has been considered. A complete response to those arguments is listed here below:

Regarding independent claims 1, 11, 24, 25, 33, and 36, Appellants assert that the combination of Weale and Guidash '804 fails to teach or suggest that the charge stored in a first storage node and the charge stored in a second storage node are collected from the same integration period. Appellants assert that “the present specification teaches that one integration period ends and the next integration period begins when the photosensitive element 302 is reset.” Appellants cite paragraph [0031] of the Pre-Grant Publication US 2005/0157194 A1 of the present application to support this assertion.

The examiner respectfully disagrees. Paragraph [0031] of the Pre-Grant Publication of the present application does not provide an explicit definition of the term “integration period.” Paragraph [0031] does not teach that "the next integration period begins when the photosensitive element 302 is reset." Rather, paragraph [0031] merely indicates when the integration period begins. Therefore, the Examiner will apply the “plain meaning" given to the term by those of ordinary skill in the art – that an "integration period" is the time that between the exposure of incident light to a photosensor and the readout of the charges accumulated by that photosensor. This definition can be found in paragraph [0096] of Bechtel et al. (US 2008/0192132). Applying this conventional definition to Weale, the “integration period” corresponds to the “image capture cycle” in col. 19, line 53-67 of Weale. Note that Weale also applies an unconventional definition of the word “integration period" in order to describe separate

time periods *within* a single image capture cycle. Also note that the single image capture cycle of Weale produces only a *single* image, not two images.

Referring to Weale, Figure 12 depicts a high-level block diagram of an image array and associated circuitry. Figure 1 depicts the components and circuitry of a single pixel site in the aforementioned image array. Photosite (112) generates electrical charge corresponding to the amount of light exposed to the photosite. First storage capacitor (122) stores the electrical charges generated by the photosite during a first period of the image capture cycle and second storage capacitor (142) stores the electrical charges generated by the photosite during a second period of the image capture cycle. Reset switches (116, 128, and 148) reset the photosite, first storage capacitor, and second storage capacitor, respectively, to clear the electrical charges generated or stored in the components.

Referring to col. 19, lines 53-67, Weale discusses the sequence in which charges are stored in separate first and second storage nodes in a single image capture cycle, i.e., integration period. At time $t_{RESET1}$, all components of the pixel site are reset. At time $t_{INT1}$, light is exposed to the individual photosite 112 and electrical charges are generated by the photosite in an amount corresponding to the amount of light received by the camera. At $t_{S1}$, charges generated by the photosite 112 are stored in the first storage capacitor 122. At $t_{RESET2}$, the photosite 112 and second storage capacitor 142 are reset of all charges. At $t_{INT2}$, the photosite 112 generates more charges corresponding to the amount of light received by the camera, and at $t_{S2}$, the charges are stored in the second storage capacitor 142. The charges stored in the first and second storage capacitors are then read out to form a single image at $t_{READ}$. This is the end of the single image capture cycle, i.e., integration period, as described by Weale.

Therefore, Weale teaches that the charges collected by a photosensitive element (photosite 112) during a single integration period (image capture cycle) is stored by a first storage node (first storage capacitor 122) and that charge from the same single integration period not stored by the first storage node is stored by a second storage node (second storage capacitor142). Thus, Weale anticipates this limitation recited by independent claims 1, 11, 24, 25, 33, and 36.

Appellants argue that the Examiner's construction is far too broad, because two integration periods cannot be fairly construed as one.

However, the examiner respectfully disagrees. Referring to the preceding response to Appellant's arguments, a conventional definition of integration period is applied and is taken to mean a time period wherein a photosite is exposed to capture a single image.

Appellants further argue that the purpose of Weale is "to collect and store two or more frames worth of data and then subsequently read these frames out at a subsequent point in time," which necessarily requires storing charge from a first integration period on a first storage node and charge from a second integration period on a second storage node.

However, the examiner respectfully disagrees. Referring to the preceding response to Appellant's arguments, a conventional definition of integration period is applied and is taken to mean a time period wherein a photosite is exposed to capture a single image. The charges stored by the first and second storage capacitors of Weale (122 and 142) are collected during different time periods within the image capture cycle, i.e., integration period, as discussed in col. 19, lines 53-67.

Appellant argues that claims 3, 5, 7, 8, 13, 15, 17, 18, and 26 are allowable for being dependent upon an allowable claim and reciting additional features. No particular arguments regarding these additional features are provided other than what the claim recites. Accordingly, claims 3, 5, 7, 8, 13, 15, 17, 18, and 26 are not believed to be allowable as set forth in the Final rejection and preceding response to the Appellant's arguments for independent claims 1, 11, 24, 25, 33, and 36.

Appellant argues that claims 36, 37, 39, 41, 44, and 45 are allowable for being dependent upon an allowable claim and reciting additional features. No particular arguments regarding these additional features are provided other than what the claim recites. Accordingly, claims 36, 37, 39, 41, 44, and 45 are not believed to be allowable as set forth in the Final rejection and preceding response to the Appellant's arguments for independent claims 1, 11, 24, 25, 33, and 36.

Appellant argues that claims 38, 40, 42, and 43 are allowable for being dependent upon an allowable claim and reciting additional features. No particular arguments regarding these additional features are provided other than what the claim recites. Accordingly, claims 38, 40, 42, and 43 are not believed to be allowable as set forth in the Final rejection and preceding response to the Appellant's arguments for independent claims 1, 11, 24, 25, 33, and 36.

**(11) Related Proceeding(s) Appendix**

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Chia-Wei Andrew Chen

/Chia-Wei A Chen/

Examiner, Art Unit 2622

Conferees:

*/Ngoc-Yen Vu/*
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*Art Unit 2622*

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